WHAT IS CLAIMED IS:

1. A semiconductor unit having two device terminals every one input/output signal, said semiconductor unit comprising:

a laminated substrate comprising at least two wiring layers which include a signal wiring layer and a power-supply or ground wiring layer, said laminated substrate having a main surface; and

a semiconductor chip having an input/output pad and being mounted on the main surface of said laminated substrate through said input/output pad,

said two device terminals being mounted on said laminated substrate and being connected to both ends of a signal wire in said signal wiring layer, said signal wire being connected to the input/output pad of said semiconductor chip through a via hole.

2. A semiconductor unit as claimed in claim 1, wherein said semiconductor chip comprises an input/output circuit corresponding to said input/output pad, said input/output circuit comprising at least one of an input buffer and an output buffer, an input protection resistor, and an electrostatic protection element.

3. A semiconductor unit having two device terminals every one input/output signal, said semiconductor unit comprising:

a laminated substrate comprising at least two wiring layers which include a signal wiring layer and a power-supply or ground wiring layer, said laminated substrate having a main surface; and

a semiconductor chip having an input/output pad and being mounted on the main surface of said laminated substrate through said input/output pad,

said semiconductor having an intra-chip wire and two input/output pads connected to both ends of said intra-chip wiring, said two device terminals being connected to said two input/output pads through two corresponding signal wires in said signal wiring layer and via holes, respectively.

4. A semiconductor unit as claimed in claim 3, wherein said semiconductor chip comprises an input/output circuit corresponding to said two input/output pads, said input/output circuit comprising at least one of an input buffer and an output buffer, an input protection resistor, and an electrostatic protection element, said input/output circuit being connected to said intra-chip wire through a different intra-chip wire.

5. A semiconductor unit as claimed in claim 1, wherein said signal wiring layer forms a micro-strip line with the ground wiring layer in said laminated substrate, said ground wiring layer being disposed between said signal wiring layer and said semiconductor chip.

6. A semiconductor unit as claimed in claim 3, wherein said signal wiring layer forms a micro-strip line with the ground wiring layer in said laminated substrate, said ground wiring layer being disposed between said signal wiring layer and said semiconductor chip.

7. A semiconductor unit as claimed in claim 1, wherein said signal wiring layer being sandwiched between the power-supply layer and the ground layer in said laminated substrate, said signal wiring layer forming a strip line with the power-supply layer or the ground layer.

8. A semiconductor unit as claimed in claim 3, wherein said signal wiring layer being sandwiched between the power-supply layer and the ground layer in said laminated substrate, said signal wiring layer forming a strip line with the power-supply layer or the ground layer.

9. A semiconductor unit as claimed in claim 1, wherein said laminated substrate has a size larger than a plan size of said semiconductor chip, said laminated substrate having a main surface and a back surface, said two device terminal being formed on the back surface of said laminated substrate, said semiconductor unit further comprising other two terminals formed on the main surface of said laminated substrate opposite to said two device terminals.

10. A semiconductor unit as claimed in claim 3, wherein said laminated

substrate has a size larger than a plan size of said semiconductor chip, said laminated substrate having a main surface and a back surface, said two device terminal being formed on the back surface of said laminated substrate, said semiconductor unit further comprising other two terminals formed on the main surface of said laminated substrate opposite to said two device terminals.

11. A semiconductor unit as claimed in claim 2, wherein said semiconductor unit is operable in response to a clock signal, a distance L between said input/output circuit and said signal wire being satisfied to a cycle time tck of the clock signal determined by a product specification of said semiconductor unit with a relationship as follows:

$2 \times 2L \times 7ns/m < tck/10$.

12. A semiconductor unit as claimed in claim 4, wherein said semiconductor unit is operable in response to a clock signal, a distance L between said input/output circuit and said signal wire being satisfied to a cycle time tck of the clock signal determined by a product specification of said semiconductor unit with a relationship as follows:

$2 \times 2L \times 7ns/m < tck/10$.

13. A semiconductor module comprising:

a module substrate comprising a connector and intra-module wires connected to said connector, said module substrate having a main surface and a back surface; and

a plurality of semiconductor units being mounted on the main surface and the back surface of said module substrate, respectively, said plurality of semiconductor units being connected to said intra-module wires,

each of said semiconductor units having two device terminals every one input/output signal, each of said semiconductor units comprising:

a laminated substrate comprising at least two wiring layers which include a signal wiring layer and a power-supply or ground wiring layer, said laminated substrate having a main surface; and

a semiconductor chip having an input/output pad and being mounted on the main surface of said laminated substrate through said input/output pad,

said two device terminals being mounted on said laminated substrate and being connected to both ends of a signal wire in said signal wiring layer, said signal wire being connected to the input/output pad of said semiconductor chip through a via hole,

one pair of said two device terminals in two semiconductor units disposed on the main surface and the back surface of said module substrate opposite to each other being connected to each other through a via hole, another pair of said two device terminals in the two semiconductor units disposed on the main surface and the back surface of said module substrate opposite to each other being connected to said connector through intra-module wires disposed in the main surface and the back surface of said module substrate, respectively.

14. A semiconductor module as claimed in claim 13, wherein said semiconductor chip comprises an input/output circuit corresponding to said input/output pad, said input/output circuit comprising at least one of an input buffer and an output buffer, an input protection resistor, and an electrostatic protection element.

15. A semiconductor module comprising:

a module substrate comprising a connector and intra-module wires connected to said connector, said module substrate having a main surface and a back surface; and

a plurality of semiconductor units being mounted on the main surface and the back surface of said module substrate, respectively, said plurality of semiconductor units being connected to said intra-module wires,

each of said semiconductor units having two device terminals every one input/output signal, each of said semiconductor units comprising:

a laminated substrate comprising at least two wiring layers which include a signal wiring layer and a power-supply or ground wiring layer, said

laminated substrate having a main surface; and

a semiconductor chip having an input/output pad and being mounted on the main surface of said laminated substrate through said input/output pad,

said semiconductor chip having an intra-chip wiring and two input/output pads connected to both ends of said intra-chip wiring, said two device terminals being connected to said two input/output pads through two corresponding signal wires in said signal wiring layer and via holes, respectively,

one pair of said two device terminals in two semiconductor units disposed on the main surface and the back surface of said module substrate opposite to each other being connected to each other through a via hole, another pair of said two device terminals in the two semiconductor units disposed on the main surface and the back surface of said module substrate opposite to each other being connected to said connector through intra-module wires disposed in the main surface and the back surface of said module substrate, respectively.

16. A semiconductor module as claimed in claim 15, wherein said semiconductor chip comprises an input/output circuit corresponding to said two input/output pads, said input/output circuit comprising at least one of an input buffer and an output buffer, an input protection resistor, and an electrostatic protection element, said input/output circuit being connected to said intra-chip wire through a different intra-chip wire.

17. A semiconductor module as claimed in claim 13, wherein said signal wiring layer forms a micro-strip line with the ground wiring layer in said laminated substrate, said ground wiring layer being disposed between said signal wiring layer and said semiconductor chip.

18. A semiconductor module as claimed in claim 15, wherein said signal wiring layer forms a micro-strip line with the ground wiring layer in said laminated substrate, said ground wiring layer being disposed between said signal wiring layer and said semiconductor chip.

19. A semiconductor module as claimed in claim 13, wherein said

signal wiring layer being sandwiched between the power-supply layer and the ground layer in said laminated substrate, said signal wiring layer forming a strip line with the power-supply layer or the ground layer.

20. A semiconductor module as claimed in claim 15, wherein said signal wiring layer being sandwiched between the power-supply layer and the ground layer in said laminated substrate, said signal wiring layer forming a strip line with the power-supply layer or the ground layer.

21. A semiconductor module as claimed in claim 13, wherein said laminated substrate has a size larger than a plan size of said semiconductor chip, said laminated substrate having a main surface and a back surface, said two device terminal being formed on the back surface of said laminated substrate, said semiconductor unit further comprising other two terminals formed on the main surface of said laminated substrate opposite to said two device terminals.

22. A semiconductor module as claimed in claim 15, wherein said laminated substrate has a size larger than a plan size of said semiconductor chip, said laminated substrate having a main surface and a back surface, said two device terminal being formed on the back surface of said laminated substrate, said semiconductor unit further comprising other two terminals formed on the main surface of said laminated substrate opposite to said two device terminals.

23. A semiconductor module as claimed in claim 14, wherein said semiconductor unit is operable in response to a clock signal, a distance L between said input/output circuit and said signal wire being satisfied to a cycle time tck of the clock signal determined by a product specification of said semiconductor unit with a relationship as follows:

$2 \times 2L \times 7ns/m < tck/10$.

24. A semiconductor module as claimed in claim 16, wherein said semiconductor unit is operable in response to a clock signal, a distance L between said input/output circuit and said signal wire being satisfied to a cycle time tck of the clock signal determined by a product specification of said

semiconductor unit with a relationship as follows:

$2 \times 2L \times 7ns/m < tck/10$.

25. A semiconductor module as claimed in claim 13, wherein said module substrate comprises at least two wiring layers.

26. A semiconductor module as claimed in claim 15, wherein said module substrate comprises at least two wiring layers.

27. A semiconductor module comprising:

a module substrate comprising a connector and an intra-module wiring connected to said connector, said module substrate having a main surface and a back surface; and

a plurality of semiconductor units mounted on the main surface and the back surface of said module substrate, respectively,

each of said semiconductor units having two upper device terminals and two lower device terminals every one input/output signal, each of said semiconductor units comprising:

a laminated substrate comprising at least two wiring layers including a signal wiring layer and a power-supply or a ground wiring layer, said laminated substrate having a main surface and a back surface; and

a semiconductor chip having an input/output pad, said semiconductor chip being mounted on the main surface of said laminated substrate, said laminated substrate having a size larger than a chip size of semiconductor chip,

said two lower device terminals being formed on the back surface of said laminated substrate, said two lower device terminals being connected to both ends of a signal wiring in said signal wiring layer, said signal wire being connected to the input/output pad of said semiconductor chip through a via hole, said two upper device terminals being formed on the main surface of said laminated substrate opposite to said two lower device terminals,

said plurality of semiconductor units being laminated, the lower device terminal formed on the back surface of said semiconductor unit of an upper layer

being connected to or being in common with the upper device terminal formed on the main surface of said semiconductor unit of a lower layer.

28. A semiconductor module comprising:

a module substrate comprising a connector and an intra-module wiring connected to said connector, said module substrate having a main surface and a back surface; and

a plurality of semiconductor units mounted on the main surface and the back surface of said module substrate, respectively,

each of said semiconductor units having two upper device terminals and two lower device terminals every one input/output signal, each of said semiconductor units comprising:

a laminated substrate comprising at least two wiring layers including a signal wiring layer and a power-supply or a ground wiring layer, said laminated substrate having a main surface and a back surface; and

a semiconductor chip having an input/output pad, said semiconductor chip being mounted on the main surface of said laminated substrate, said laminated substrate having a size larger than a chip size of semiconductor chip,

said semiconductor chip comprising an intra-chip wire and two input/output pads connected to both ends of said intra-chip wire,

said two lower device terminals being formed on the back surface of said laminated substrate, said two lower device terminals being connected to said two input/output pads through corresponding signal wires in said signal wiring layer and via holes, respectively, said two upper device terminals being formed on the main surface of said laminated substrate opposite to said two lower device terminals,

said plurality of semiconductor units being laminated, the lower device terminal formed on the back surface of said semiconductor unit of an upper layer being connected to or being in common with the upper device terminal formed on the main surface of said semiconductor unit of a lower layer.

29. A semiconductor module as claimed in claim 27, wherein one pair of said two lower device terminals in two semiconductor units disposed on the main surface and the back surface of said module substrate opposite to each other are connected to each other through a via hole, another pair of said two lower device terminals in the two semiconductor units disposed on the main surface and the back surface of said module substrate opposite to each other being connected to said connector through intra-module wires disposed in the main surface and the back surface of said module substrate, respectively.

30. A semiconductor module as claimed in claim 28, wherein one pair of said two lower device terminals in two semiconductor units disposed on the main surface and the back surface of said module substrate opposite to each other are connected to each other through a via hole, another pair of said two lower device terminals in the two semiconductor units disposed on the main surface and the back surface of said module substrate opposite to each other being connected to said connector through intra-module wires disposed in the main surface and the back surface of said module substrate, respectively.

31. A semiconductor module as claimed in claim 13, wherein said semiconductor units comprise memory devices.

32. A semiconductor module as claimed in claim 15, wherein said semiconductor units comprise memory devices.

33. A semiconductor module as claimed in claim 27, wherein said semiconductor units comprise memory devices.

34. A semiconductor module as claimed in claim 28, wherein said semiconductor units comprise memory devices.

35. A semiconductor module as claimed in claim 31, wherein said semiconductor module further comprises a register, a control wiring between said register and a plurality of memory devices passing through between said two device terminals.

36. A semiconductor module as claimed in claim 32, wherein said

semiconductor module further comprises a register, a control wire between said register and a plurality of memory devices passing through between said two device terminals.

37. A semiconductor module as claimed in claim 33, wherein said semiconductor module further comprises a register, a control wire between said register and a plurality of memory devices passing through between said two lower device terminals.

38. A semiconductor module as claimed in claim 34, wherein said semiconductor module further comprises a register, a control wire between said register and a plurality of memory devices passing through between said two lower device terminals.

39. A memory system comprising:

a mother board having mother board wires;

a controller mounted on said mother board;

a plurality of semiconductor modules mounted on said mother board in turn, said plurality of semiconductor modules being connected to said controller through said mother board wires in turn; and

terminating resistors connected to terminations of said mother board wires,

each of said semiconductor modules comprising:

a module substrate comprising a connector and intra-module wires connected to said connector, said module substrate having a main surface and a back surface; and

a plurality of memory devices being mounted on the main surface and the back surface of said module substrate, respectively, said plurality of memory devices being connected to said intra-module wires,

each of said memory devices having two device terminals every one input/output signal, each of said memory devices comprising:

a laminated substrate comprising at least two wiring layers which

include a signal wiring layer and a power-supply or ground wiring layer, said laminated substrate having a main surface; and

a semiconductor chip having an input/output pad and being mounted on the main surface of said laminated substrate through said input/output pad,

said two device terminals being mounted on said laminated substrate and being connected to both ends of a signal wire in said signal wiring layer, said signal wiring being connected to the input/output pad of said semiconductor chip through a via hole,

one pair of said two device terminals in two memory devices disposed on the main surface and the back surface of said module substrate opposite to each other being connected to each other through a via hole, another pair of said two device terminals in the two memory devices disposed on the main surface and the back surface of said module substrate opposite to each other being connected to said connector through intra-module wires disposed in the main surface and the back surface of said module substrate, respectively,

each of said mother board wires being connected through said intra-module wires in a chain fashion.

40. A memory system comprising:

a mother board having mother board wires;

a controller mounted on said mother board;

a plurality of semiconductor modules mounted on said mother board in turn, said plurality of semiconductor modules being connected to said controller through said mother board wires in turn; and

terminating resistors connected to terminations of said mother board wires,

each of said semiconductor modules comprising:

a module substrate comprising a connector and intra-module wires connected to said connector, said module substrate having a main surface and a back surface; and

a plurality of memory devices being mounted on the main surface and the back surface of said module substrate, respectively, said plurality of memory devices being connected to said intra-module wires,

each of said memory devices having two device terminals every one input/output signal, each of said memory devices comprising:

a laminated substrate comprising at least two wiring layers which include a signal wiring layer and a power-supply or ground wiring layer, said laminated substrate having a main surface; and

a semiconductor chip having an input/output pad and being mounted on the main surface of said laminated substrate through said input/output pad,

said semiconductor chip having an intra-chip wire and two input/output pads connected to both ends of said intra-chip wire, said two device terminals being connected to said two input/output pads through two corresponding signal wires in said signal wiring layer and via holes, respectively,

one pair of said two device terminals in two memory devices disposed on the main surface and the back surface of said module substrate opposite to each other being connected to each other through a via hole, another pair of said two device terminals in the two memory devices disposed on the main surface and the back surface of said module substrate opposite to each other being connected to said connector through intra-module wires disposed in the main surface and the back surface of said module substrate, respectively,

each of said mother board wires being connected through said intra-module wires in a chain fashion.

41. A memory system comprising:

a mother board having mother board wires;

a controller mounted on said mother board;

a plurality of semiconductor modules mounted on said mother board in turn, said plurality of semiconductor modules being connected to said controller through said mother board wires in turn; and

terminating resistors connected to terminations of said mother board wires,

each of said semiconductor modules comprising:

a module substrate comprising a connector and an intra-module wire connected to said connector, said module substrate having a main surface and a back surface; and

a plurality of memory devices mounted on the main surface and the back surface of said module substrate, respectively,

each of said memory devices having two upper device terminals and two lower device terminals every one input/output signal, each of said memory devices comprising:

a laminated substrate comprising at least two wiring layers including a signal wiring layer and a power-supply or a ground wiring layer, said laminated substrate having a main surface and a back surface; and

a semiconductor chip having an input/output pad, said semiconductor chip being mounted on the main surface of said laminated substrate, said laminated substrate having a size larger than a chip size of semiconductor chip,

said two lower device terminals being formed on the back surface of said laminated substrate, said two lower device terminals being connected to both ends of a signal wiring in said signal wiring layer, said signal wiring being connected to the input/output pad of said semiconductor chip through a via hole, said two upper device terminals being formed on the main surface of said laminated substrate opposite to said two lower device terminals,

said plurality of memory devices being laminated, the lower device terminal formed on the back surface of said memory device of an upper layer being connected to or being in common with the upper device terminal formed on the main surface of said memory device of a lower layer,

each of said mother board wires being connected through said intra-module wires in a chain fashion.

42. A memory system comprising:

a mother board having mother board wires;

a controller mounted on said mother board;

a plurality of semiconductor modules mounted on said mother board in turn, said plurality of semiconductor modules being connected to said controller through said mother board wires in turn; and

terminating resistors connected to terminations of said mother board wires,

each of said semiconductor modules comprising:

a module substrate comprising a connector and an intra-module wire connected to said connector, said module substrate having a main surface and a back surface; and

a plurality of memory devices mounted on the main surface and the back surface of said module substrate, respectively,

each of said memory devices having two upper device terminals and two lower device terminals every one input/output signal, each of said memory devices comprising:

a laminated substrate comprising at least two wiring layers including a signal wiring layer and a power-supply or a ground wiring layer, said laminated substrate having a main surface and a back surface; and

a semiconductor chip having an input/output pad, said semiconductor chip being mounted on the main surface of said laminated substrate, said laminated substrate having a size larger than a chip size of semiconductor chip,

said semiconductor chip comprising an intra-chip wire and two input/output pads connected to both ends of said intra-chip wire,

said two lower device terminals being formed on the back surface of said laminated substrate, said two lower device terminals being connected to said two input/output pads through corresponding signal wires in said signal wiring layer and via holes, respectively, said two upper device terminals being

formed on the main surface of said laminated substrate opposite to said two lower device terminals,

said plurality of memory devices being laminated, the lower device terminal formed on the back surface of said memory device of an upper layer being connected to or being in common with the upper device terminal formed on the main surface of said memory device of a lower layer,

each of said mother board wires being connected through said intra-module wires in a chain fashion.

43. A memory system comprising:

a mother board having mother board wires;

a controller mounted on said mother board;

a plurality of semiconductor modules mounted on said mother board in turn, said plurality of semiconductor modules being connected to said controller through said mother board wires in turn; and

terminating resistors connected to terminations of said mother board wires,

each of said semiconductor modules comprising:

a module substrate comprising a connector and intra-module wires connected to said connector, said module substrate having a main surface and a back surface;

a plurality of memory devices being mounted on the main surface and the back surface of said module substrate, respectively, said plurality of memory devices being connected to said intra-module wires; and

a resister mounted on said module substrate, a control wiring between said resister and said plurality of memory devices passing through between said two device terminals,

each of said memory devices having two device terminals every one input/output signal, each of said memory devices comprising:

a laminated substrate comprising at least two wiring layers which

include a signal wiring layer and a power-supply or ground wiring layer, said laminated substrate having a main surface; and

a semiconductor chip having an input/output pad and being mounted on the main surface of said laminated substrate through said input/output pad,

said two device terminals being mounted on said laminated substrate and being connected to both ends of a signal wiring in said signal wiring layer, said signal wiring being connected to the input/output pad of said semiconductor chip through a via hole,

one pair of said two device terminals in two memory devices disposed on the main surface and the back surface of said module substrate opposite to each other being connected to each other through a via hole, another pair of said two device terminals in the two memory devices disposed on the main surface and the back surface of said module substrate opposite to each other being connected to said connector through intra-module wires disposed in the main surface and the back surface of said module substrate, respectively,

each of said mother board wires being connected through said intra-module wires in a chain fashion.

44. A memory system comprising:

a mother board having mother board wires;

a controller mounted on said mother board;

a plurality of semiconductor modules mounted on said mother board in turn, said plurality of semiconductor modules being connected to said controller through said mother board wires in turn; and

terminating resistors connected to terminations of said mother board wires,

each of said semiconductor modules comprising:

a module substrate comprising a connector and intra-module wires connected to said connector, said module substrate having a main surface and a back surface;

a plurality of memory devices being mounted on the main surface and the back surface of said module substrate, respectively, said plurality of memory devices being connected to said intra-module wires; and

a resister mounted on said module substrate, a control wiring between said resister and said plurality of memory devices passing through between said two device terminals,

each of said memory devices having two device terminals every one input/output signal, each of said memory devices comprising:

a laminated substrate comprising at least two wiring layers which include a signal wiring layer and a power-supply or ground wiring layer, said laminated substrate having a main surface; and

a semiconductor chip having an input/output pad and being mounted on the main surface of said laminated substrate through said input/output pad,

said semiconductor chip having an intra-chip wiring and two input/output pads connected to both ends of said intra-chip wire, said two device terminals being connected to said two input/output pads through two corresponding signal wires in said signal wiring layer and via holes, respectively,

one pair of said two device terminals in two memory devices disposed on the main surface and the back surface of said module substrate opposite to each other being connected to each other through a via hole, another pair of said two device terminals in the two memory devices disposed on the main surface and the back surface of said module substrate opposite to each other being connected to said connector through intra-module wires disposed in the main surface and the back surface of said module substrate, respectively,

each of said mother board wires being connected through said intra-module wires in a chain fashion.

45. A memory system comprising:

a mother board having mother board wires;

a controller mounted on said mother board;

a plurality of semiconductor modules mounted on said mother board in turn, said plurality of semiconductor modules being connected to said controller through said mother board wires in turn; and

terminating resistors connected to terminations of said mother board wires,

each of said semiconductor modules comprising:

a module substrate comprising a connector and an intra-module wire connected to said connector, said module substrate having a main surface and a back surface;

a plurality of memory devices mounted on the main surface and the back surface of said module substrate, respectively, each of said memory devices having two upper device terminals and two lower device terminals every one input/output signal; and

a register mounted on said module substrate, a control wire between said register and said plurality of memory devices passing through between said two lower device terminals,

each of said memory devices comprising:

a laminated substrate comprising at least two wiring layers including a signal wiring layer and a power-supply or a ground wiring layer, said laminated substrate having a main surface and a back surface; and

a semiconductor chip having an input/output pad, said semiconductor chip being mounted on the main surface of said laminated substrate, said laminated substrate having a size larger than a chip size of semiconductor chip,

said two lower device terminals being formed on the back surface of said laminated substrate, said two lower device terminals being connected to both ends of a signal wire in said signal wiring layer, said signal wire being connected to the input/output pad of said semiconductor chip through a via hole, said two upper device terminals being formed on the main surface of said laminated substrate opposite to said two lower device terminals,

said plurality of memory devices being laminated, the lower device terminal formed on the back surface of said memory device of an upper layer being connected to or being in common with the upper device terminal formed on the main surface of said memory device of a lower layer,

each of said mother board wires being connected through said intra-module wires in a chain fashion.

46. A memory system comprising:

a mother board having mother board wires;

a controller mounted on said mother board;

a plurality of semiconductor modules mounted on said mother board in turn, said plurality of semiconductor modules being connected to said controller through said mother board wires in turn; and

terminating resistors connected to terminations of said mother board wires,

each of said semiconductor modules comprising:

a module substrate comprising a connector and an intra-module wire connected to said connector, said module substrate having a main surface and a back surface;

a plurality of memory devices mounted on the main surface and the back surface of said module substrate, respectively, each of said memory devices having two upper device terminals and two lower device terminals every one input/output signal; and

a register mounted on said module substrate, a control wire between said register and said plurality of memory devices passing through between said two lower device terminals,

each of said memory devices comprising:

a laminated substrate comprising at least two wiring layers including a signal wiring layer and a power-supply or a ground wiring layer, said laminated substrate having a main surface and a back surface; and

a semiconductor chip having an input/output pad, said semiconductor chip being mounted on the main surface of said laminated substrate, said laminated substrate having a size larger than a chip size of said semiconductor chip,

said semiconductor chip comprising an intra-chip wire and two input/output pads connected to both ends of said intra-chip wire,

said two lower device terminals being formed on the back surface of said laminated substrate, said two lower device terminals being connected to said two input/output pads through corresponding signal wires in said signal wiring layer and via holes, respectively, said two upper device terminals being formed on the main surface of said laminated substrate opposite to said two lower device terminals,

said plurality of memory devices being laminated, the lower device terminal formed on the back surface of said memory device of an upper layer being connected to or being in common with the upper device terminal formed on the main surface of said memory device of a lower layer,

each of said mother board wires being connected through said intra-module wires in a chain fashion.

47. A memory system as claimed in claim 39, wherein said signal wire comprises a data bus for reading data from said memory devices and for writing data into said memory devices.

48. A memory system as claimed in claim 40, wherein said signal wire comprises a data bus for reading data from said memory devices and for writing data into said memory devices.

49. A memory system as claimed in claim 41, wherein said signal wire comprises a data bus for reading data from said memory devices and for writing data into said memory devices.

50. A memory system as claimed in claim 42, wherein said signal wire comprises a data bus for reading data from said memory devices and for writing

data into said memory devices.

51. A memory system as claimed in claim 43, wherein said signal wire comprises a data bus for reading data from said memory devices and for writing data into said memory devices.

52. A memory system as claimed in claim 44, wherein said signal wire comprises a data bus for reading data from said memory devices and for writing data into said memory devices.

53. A memory system as claimed in claim 45, wherein said signal wire comprises a data bus for reading data from said memory devices and for writing data into said memory devices.

54. A memory system as claimed in claim 46, wherein said signal wire comprises a data bus for reading data from said memory devices and for writing data into said memory devices.

55. A semiconductor unit having at least two device terminals every one input/output signal,

said semiconductor unit having said two device terminals disposed in different sides of right and left, front and rear, or inside and outside of said semiconductor unit one by one, said two device terminals being wired to an input/output pad of a semiconductor chip that corresponds to said input/output signal.

56. A semiconductor unit having two device terminals every one input/output signal,

said semiconductor unit having said two device terminals disposed in different sides of right and left of said semiconductor unit one by one, only one of said two device terminals being wired to an input/output pad of a semiconductor chip that corresponds to said input/output signal.

57. A semiconductor unit as claimed in claim 56, wherein only intra-package wire connected to said only one of said two device terminals being connected to the input/output pad of said semiconductor chip that correspond to

said input/output signal with a wire bonding.

58. A semiconductor unit as claimed in claim 56, wherein only intra-package wiring connected to said only one of said two device terminals being connected to the input/output pad of said semiconductor chip that correspond to said input/output signal with a jumper chip.

59. A semiconductor unit as claimed in claim 56, wherein said two device terminals are wired to the input/output pad of said semiconductor chip with two intra-package wire, the intra-package wire connected to one of said two device terminals being cut.

60. A semiconductor unit having two device terminals every one input/output signal, said semiconductor unit comprising:

a laminated substrate comprising at least two wiring layers including a signal wiring layer and a power-supply or a ground wiring layer, said laminated substrate having a main surface and a back surface; and

a semiconductor chip having an input/output pad, said semiconductor chip being mounted on the main surface of said laminated substrate,

said two device terminals being disposed on the main surface and the back surface of said laminated substrate opposite to each other, respectively, said two device terminals being connected to each other through a via hole, said via hole being connected to the input/output pad of said semiconductor chip through a wire.

61. A semiconductor unit having two device terminals every one input/output signal, said semiconductor unit comprising:

a laminated substrate comprising at least two wiring layers including a signal wiring layer and a power-supply or a ground wiring layer, said laminated substrate having a main surface and a back surface; and

two semiconductor chips each having an input/output pad, said semiconductor chips being mounted on the main surface and the back surface of said laminated substrate, respectively,

said two device terminals being disposed on the main surface and the back surface of said laminated substrate opposite to each other, respectively, said two device terminals being connected to each other through a via hole, said via hole being connected to the input/output pads of said two semiconductor chip through a wire.

62. A laminated semiconductor unit comprising a semiconductor unit of an upper layer and a semiconductor unit of a lower layer, each of said semiconductor unit of the upper layer and said semiconductor unit of the lower layer having two device terminals every one input/output signal, each of said semiconductor unit of the upper layer and said semiconductor unit of the lower layer comprising:

a laminated substrate comprising at least two wiring layers including a signal wiring layer and a power-supply or a ground wiring layer, said laminated substrate having a main surface and a back surface; and

a semiconductor chip having an input/output pad, said semiconductor chip being mounted on the main surface of said laminated substrate,

said two device terminals being disposed on the main surface and the back surface of said laminated substrate opposite to each other, respectively, said two device terminals being connected to each other through a via hole, said via hole being connected to the input/output pad of said semiconductor chip through a wire,

the device terminal disposed on the back surface of said semiconductor unit of the upper layer being connected to or in common with the device terminal disposed on the main surface of said semiconductor unit of the lower layer.

63. A memory module comprising a semiconductor unit having at least two device terminals every one input/output signal,

said semiconductor unit having said two device terminals disposed in different sides of right and left, front and rear, or inside and outside of said semiconductor unit one by one, said two device terminals being wired to an

input/output pad of a semiconductor chip that corresponds to said input/output signal,

a wire being made by selecting one of said two device terminals that can shortening said wire on wiring for said input/output signal.

64. A memory module comprising a semiconductor unit having two device terminals every one input/output signal,

said semiconductor unit having said two device terminals disposed in different sides of right and left of said semiconductor unit one by one, only one of said two device terminals being wired to an input/output pad of a semiconductor chip that corresponds to said input/output signal,

a wire being made by selecting one of said two device terminals that can shortening said wire on wiring for said input/output signal.

65. A memory module comprising a semiconductor unit having two device terminals every one input/output signal, said semiconductor unit comprising:

a laminated substrate comprising at least two wiring layers including a signal wiring layer and a power-supply or a ground wiring layer, said laminated substrate having a main surface and a back surface; and

a semiconductor chip having an input/output pad, said semiconductor chip being mounted on the main surface of said laminated substrate,

said two device terminals being disposed on the main surface and the back surface of said laminated substrate opposite to each other, respectively, said two device terminals being connected to each other through a via hole, said via hole being connected to the input/output pad of said semiconductor chip through a wire,

a mounting being made by selecting a surface having connection of a memory module substrate of said semiconductor unit so as to wire one of said two device terminals that can shorten a wire on wiring for said input/output signal.

66. A memory module comprising a semiconductor unit having two device terminals every one input/output signal, said semiconductor unit comprising:

a laminated substrate comprising at least two wiring layers including a signal wiring layer and a power-supply or a ground wiring layer, said laminated substrate having a main surface and a back surface; and

two semiconductor chips each having an input/output pad, said semiconductor chips being mounted on the main surface and the back surface of said laminated substrate, respectively,

said two device terminals being disposed on the main surface and the back surface of said laminated substrate opposite to each other, respectively, said two device terminals being connected to each other through a via hole, said via hole being connected to the input/output pads of said two semiconductor chip through a wire,

a mounting being made by selecting a surface having connection of a memory module substrate of said semiconductor unit so as to wire one of said two device terminals that can shorten a wire on wiring for said input/output signal.

67. A memory module comprising a laminated semiconductor unit which comprises a semiconductor unit of an upper layer and a semiconductor unit of a lower layer, each of said semiconductor unit of the upper layer and said semiconductor unit of the lower layer having two device terminals every one input/output signal, each of said semiconductor unit of the upper layer and said semiconductor unit of the lower layer comprising:

a laminated substrate comprising at least two wiring layers including a signal wiring layer and a power-supply or a ground wiring layer, said laminated substrate having a main surface and a back surface; and

a semiconductor chip having an input/output pad, said semiconductor chip being mounted on the main surface of said laminated substrate,

said two device terminals being disposed on the main surface and the back surface of said laminated substrate opposite to each other, respectively, said two device terminals being connected to each other through a via hole, said via hole being connected to the input/output pad of said semiconductor chip through a wire,

the device terminal disposed on the back surface of said semiconductor unit of the upper layer being connected to or in common with the device terminal disposed on the main surface of said semiconductor unit of the lower layer,

a mounting being made by selecting a surface having connection of a memory module substrate of said semiconductor unit so as to wire one of said two device terminals that can shorten a wire on wiring for said input/output signal.

68. A semiconductor unit as claimed in claim 61, wherein said semiconductor unit further has different four device terminals every at least one signal, first and second terminals in said different four device terminals being disposed on the main and the back surfaces of said laminated substrate at left side opposite to each other, third and fourth terminals of said different four device terminals being disposed on the main and the back surfaces of said laminated substrate at right side opposite to each other, said first and said second terminals and said third and said fourth terminals being disposed at left and right of said laminated substrate opposite to each other, said first and said second terminals being connected to each other through a first via hole, said third and said fourth terminals being connected to each other through a second via hole, said first and said second via holes being connected to a corresponding signal pad of said semiconductor chip by a wire, respectively.

69. A semiconductor unit having two device terminals every at least one input/output signal, said semiconductor unit comprising:

a laminated substrate comprising at least two wiring layers including a signal wiring layer and a power-supply or ground wiring layer, said laminated

substrate having a main surface and a back surface;

at least one semiconductor chip having an input/output pad, said semiconductor chip being mounted on one or both of said main and said back surfaces of said laminated substrate through said input/output pad,

said two device terminals being disposed on the main and said back surfaces of said laminated substrate at one side, respectively, said two device terminals being connected to each other through a via hole, said via hole being connected to the input/output pad of said semiconductor chip by a wire,

said semiconductor unit further having different four device terminals every at least different one input/output signal, first and second terminals in said different four device terminals being disposed on the main and the back surfaces of said laminated substrate at left side opposite to each other, third and fourth terminals of said different four device terminals being disposed on the main and the back surfaces of said laminated substrate at right side opposite to each other, said first and said second terminals and said third and said fourth terminals being disposed at left and right of said laminated substrate opposite to each other, said first and said second terminals being connected to each other through a first via hole, said third and said fourth terminals being connected to each other through a second via hole, said first and said second via holes being connected to a corresponding signal pad of said semiconductor chip by a wire, respectively.

70. A memory system mounting, as a memory, a semiconductor unit thereon, said semiconductor unit having two device terminals every one input/output signal, said semiconductor unit comprising:

a laminated substrate comprising at least two wiring layers including a signal wiring layer and a power-supply or a ground wiring layer, said laminated substrate having a main surface and a back surface; and

two semiconductor chips each having an input/output pad, said semiconductor chips being mounted on the main surface and the back surface of said laminated substrate, respectively,

said two device terminals being disposed on the main surface and the back surface of said laminated substrate opposite to each other, respectively, said two device terminals being connected to each other through a via hole, said via hole being connected to the input/output pads of said two semiconductor chip through a wire,

said semiconductor unit further having different four device terminals every at least one signal, first and second terminals in said different four device terminals being disposed on the main and the back surfaces of said laminated substrate at left side opposite to each other, third and fourth terminals of said different four device terminals being disposed on the main and the back surfaces of said laminated substrate at right side opposite to each other, said first and said second terminals and said third and said fourth terminals being disposed at left and right of said laminated substrate opposite to each other, said first and said second terminals being connected to each other through a first via hole, said third and said fourth terminals being connected to each other through a second via hole, said first and said second via holes being connected to a corresponding signal pad of said semiconductor chip by a wire, respectively.

71. A memory system mounting, as a memory, a semiconductor unit thereon, said semiconductor unit having two device terminals every at least one input/output signal, said semiconductor unit comprising:

a laminated substrate comprising at least two wiring layers including a signal wiring layer and a power-supply or ground wiring layer, said laminated substrate having a main surface and a back surface;

at least one semiconductor chip having an input/output pad, said semiconductor chip being mounted on one or both of said main and said back surfaces of said laminated substrate through said input/output pad,

said two device terminals being disposed on the main and said back surfaces of said laminated substrate at one side, respectively, said two device terminals being connected to each other through a via hole, said via hole being

connected to the input/output pad of said semiconductor chip by a wire,

said semiconductor unit further having different four device terminals every at least different one input/output signal, first and second terminals in said different four device terminals being disposed on the main and the back surfaces of said laminated substrate at left side opposite to each other, third and fourth terminals of said different four device terminals being disposed on the main and the back surfaces of said laminated substrate at right side opposite to each other, said first and said second terminals and said third and said fourth terminals being disposed at left and right of said laminated substrate opposite to each other, said first and said second terminals being connected to each other through a first via hole, said third and said fourth terminals being connected to each other through a second via hole, said first and said second via holes being connected to a corresponding signal pad of said semiconductor chip through a wire, respectively.

72. A semiconductor unit comprising a package having a main surface and a back surface, said package having at least two ball terminal adhesive areas every one input/output signal on the main and the back surfaces of said package, a ball terminal being adhered to only one ball terminal adhesive area on one surface of said package.

73. A memory system mounting a plurality of semiconductor units thereon, each of said semiconductor units comprising a package having a main surface and a back surface, said package having at least two ball terminal adhesive areas every one input/output signal on the main and the back surface of said package, a ball terminal being adhered in at least one of said semiconductor units to only ball terminal adhesive area so as to shorten an input/output wiring on said memory system.